

PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

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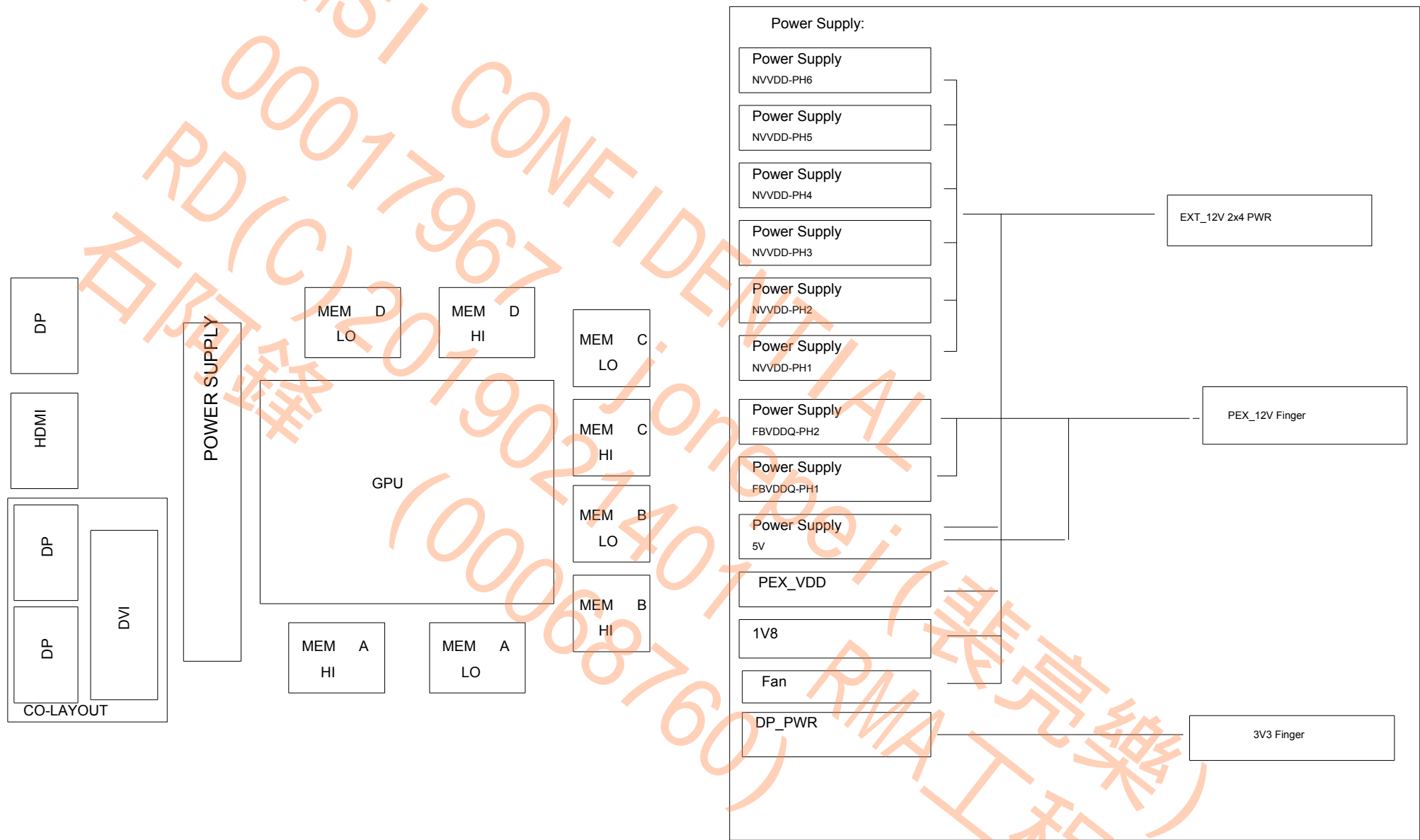
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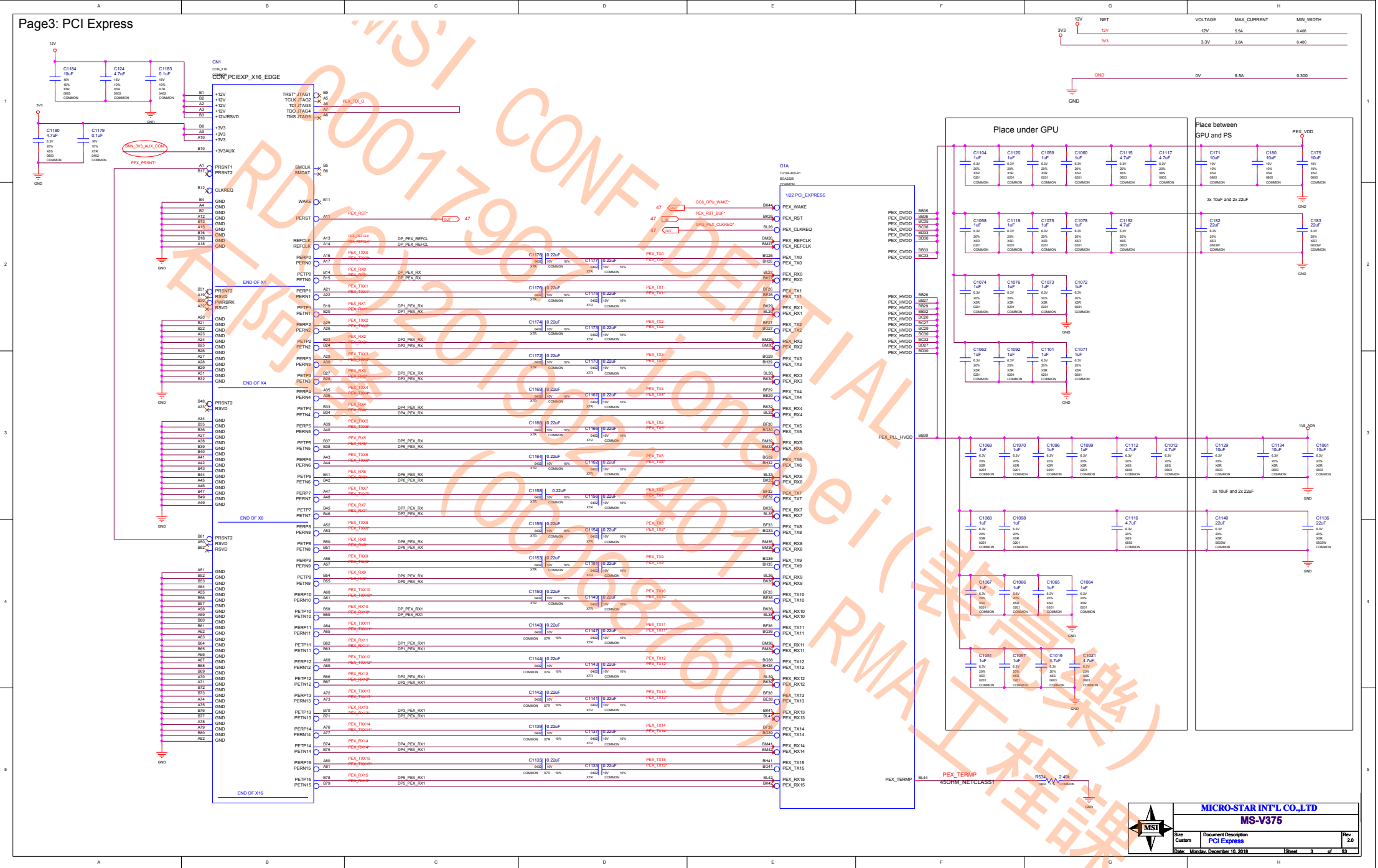
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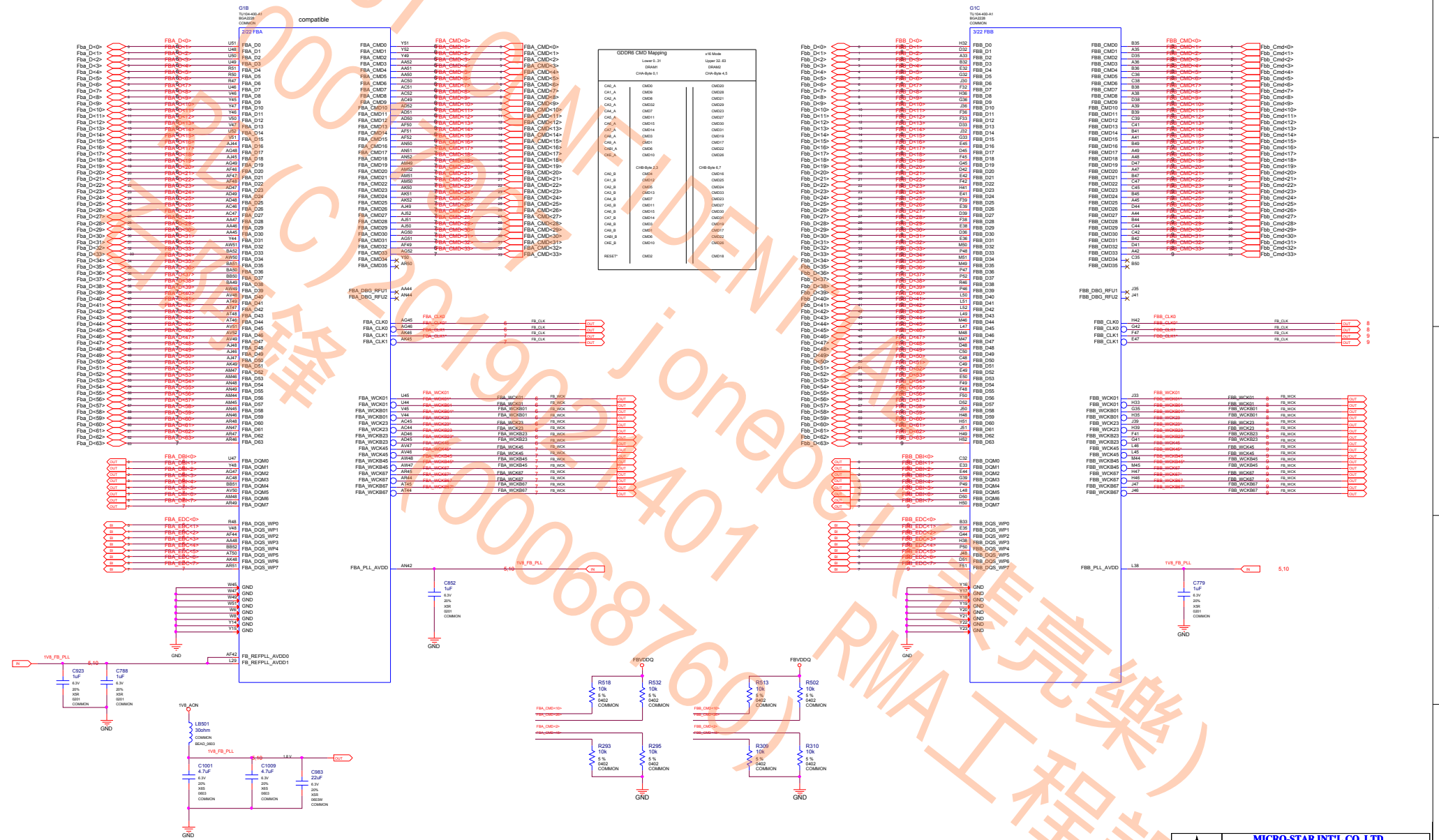
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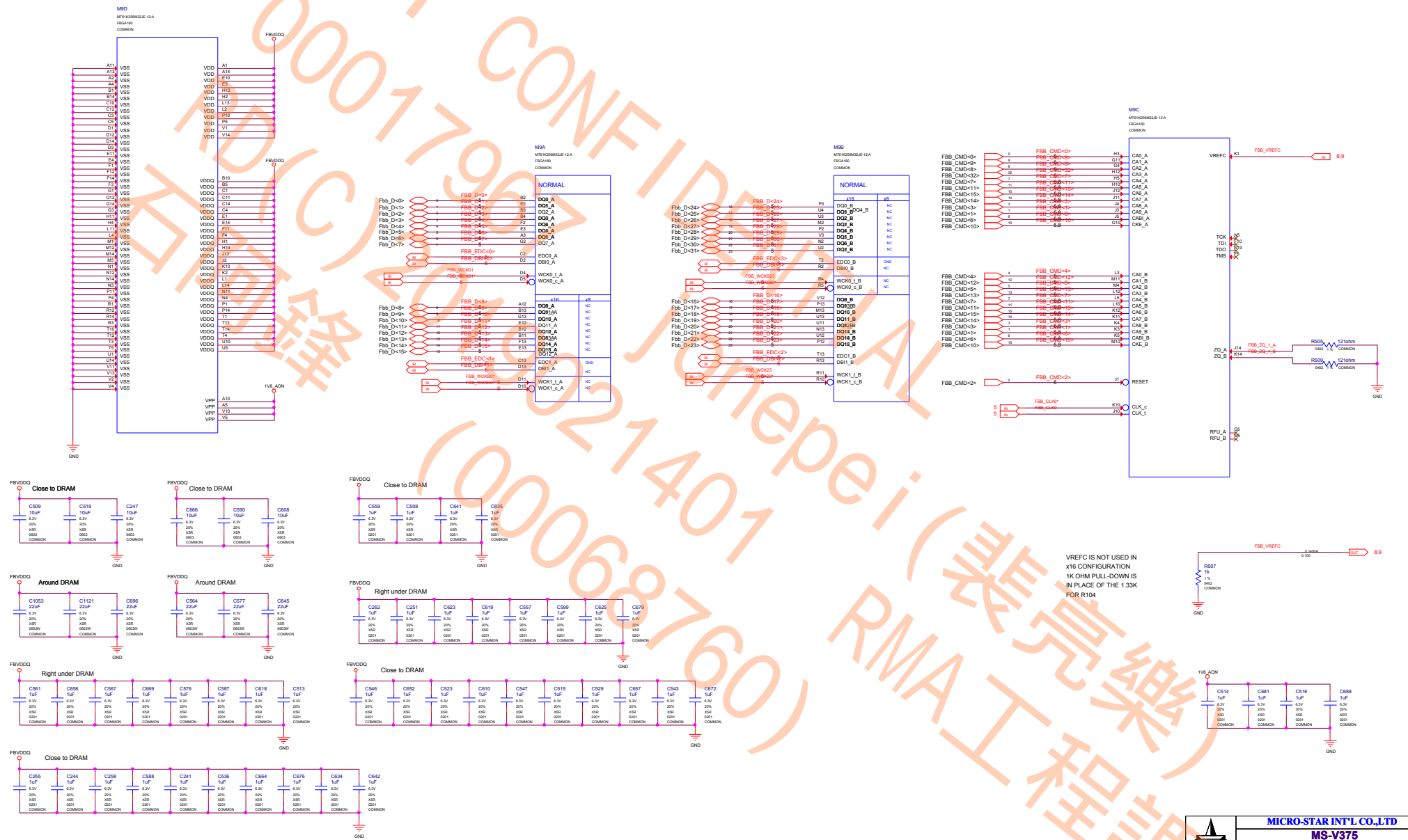


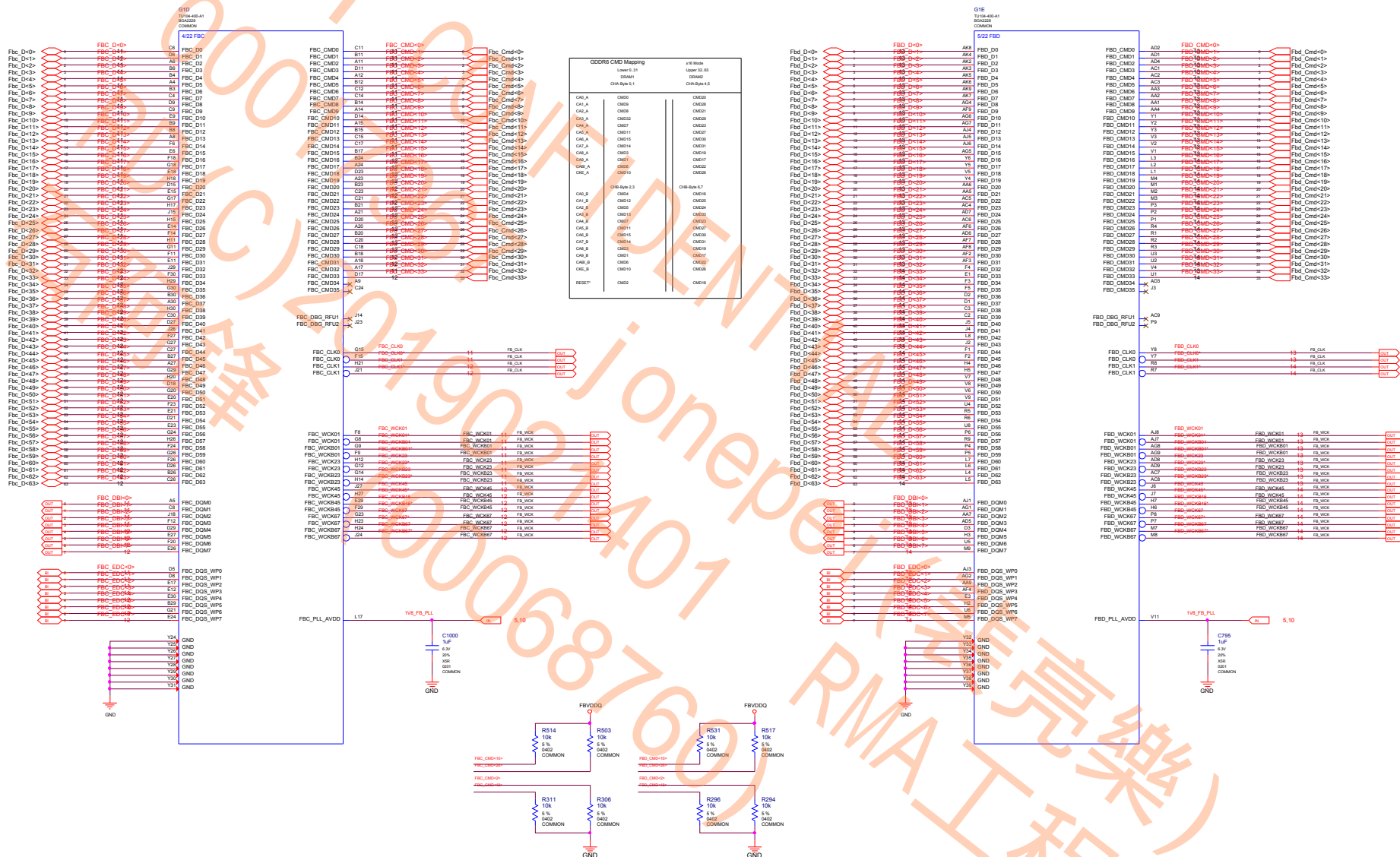


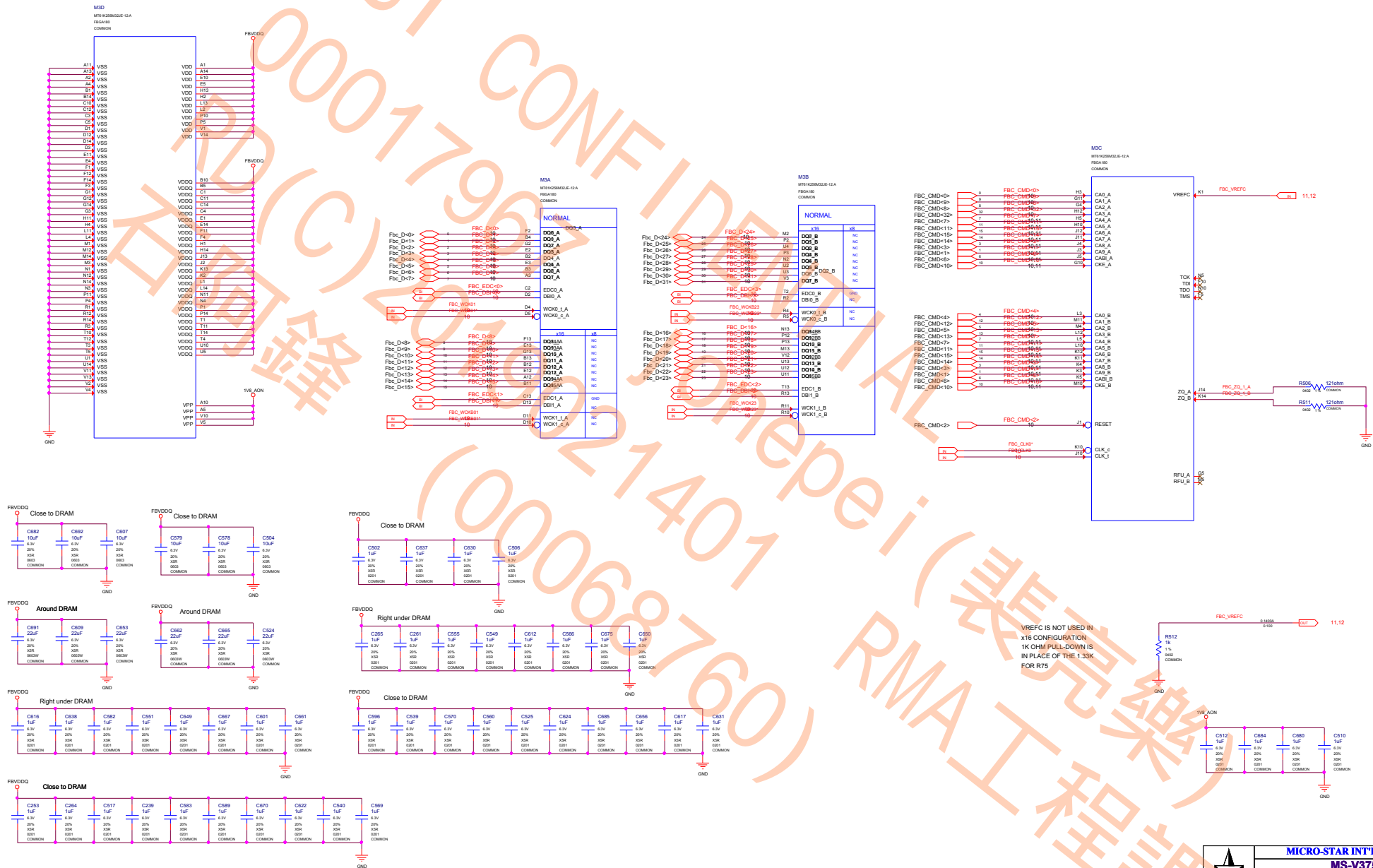
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DELETE RC TERMINATIONS

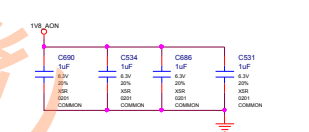
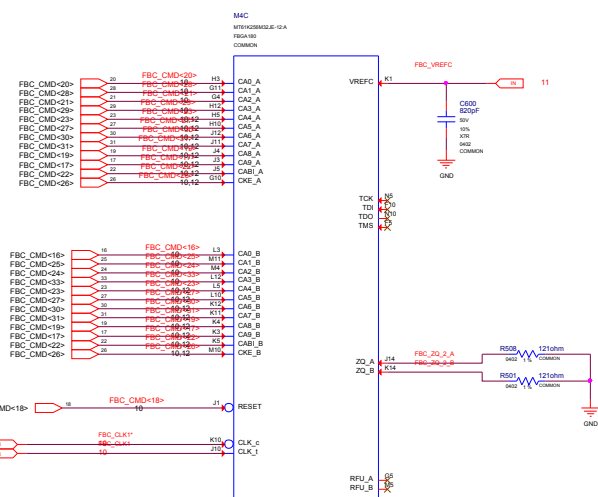
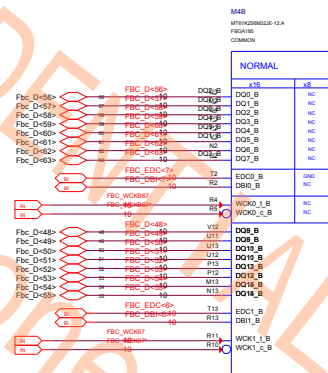
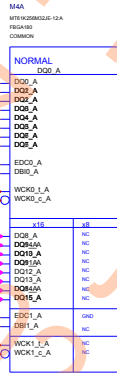
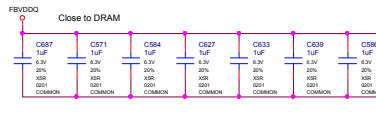
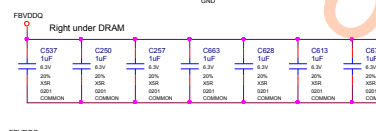
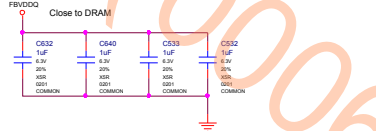
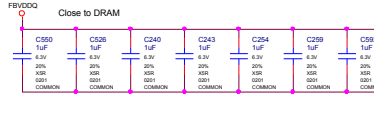
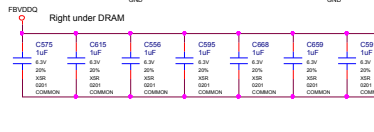
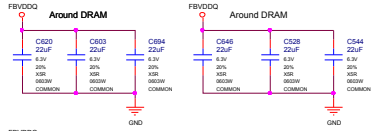
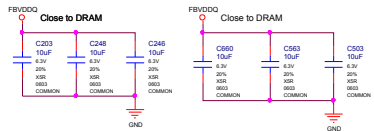
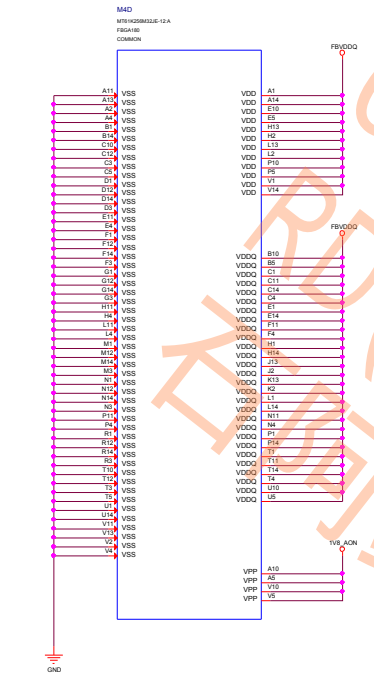
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MS-V375		
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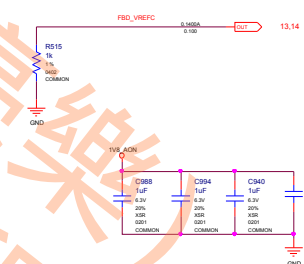
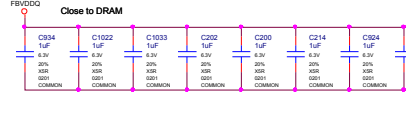
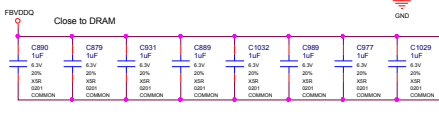
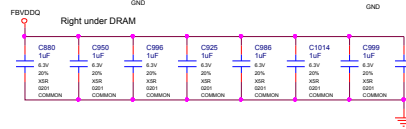
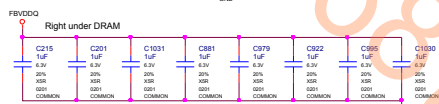
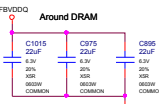
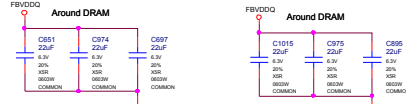
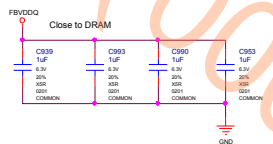
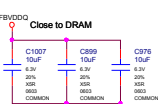
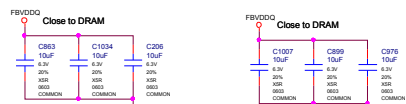
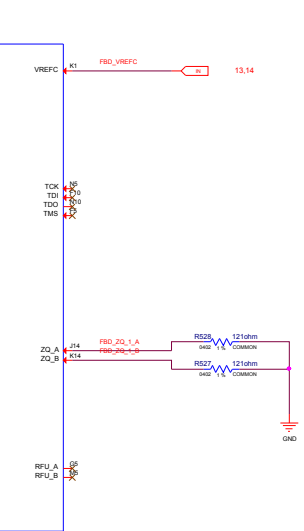
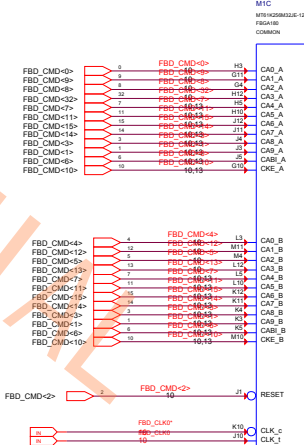
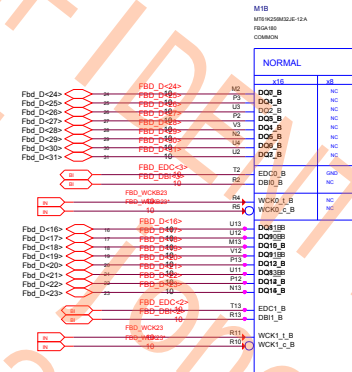
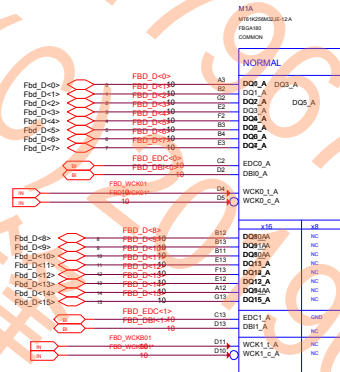




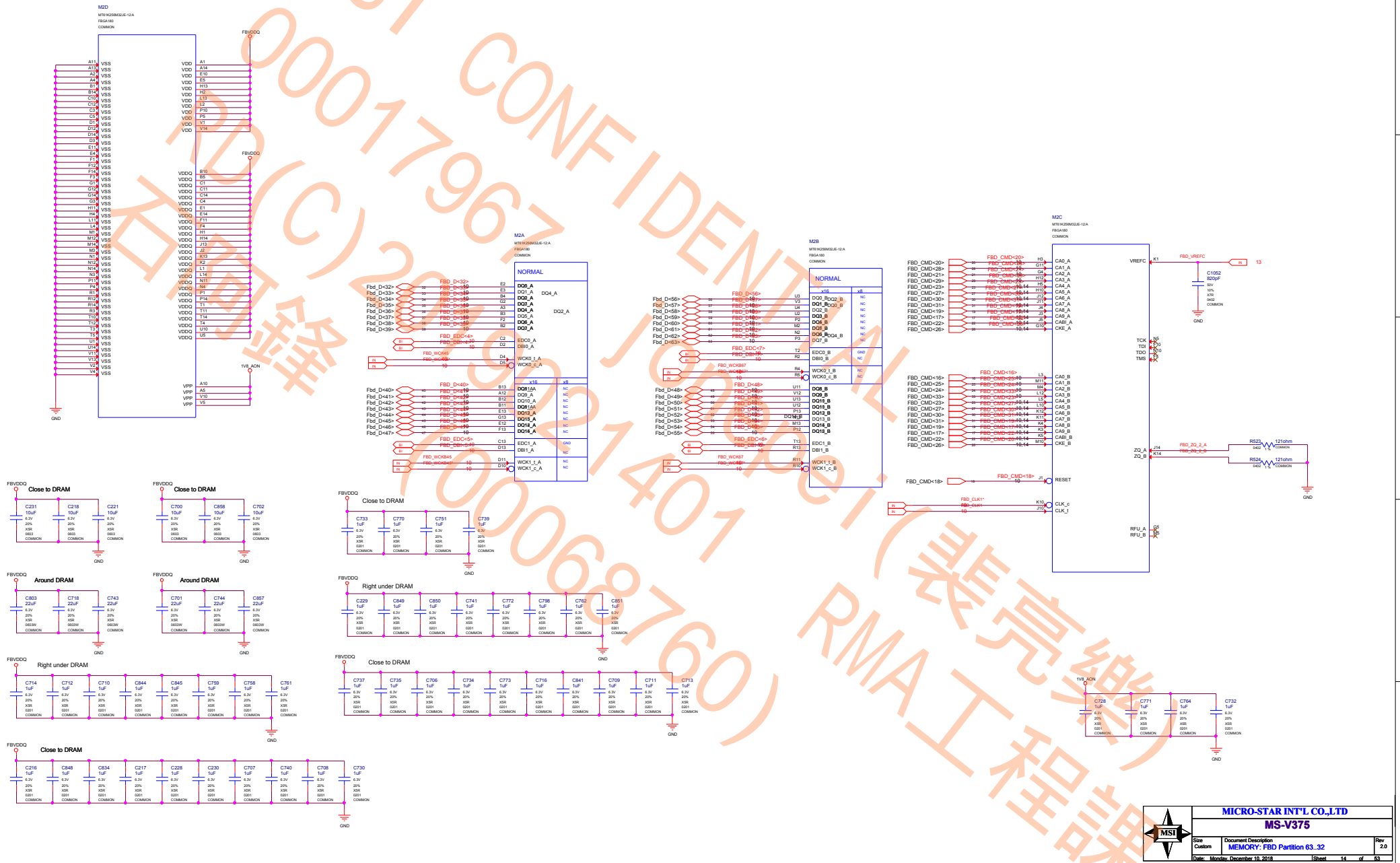


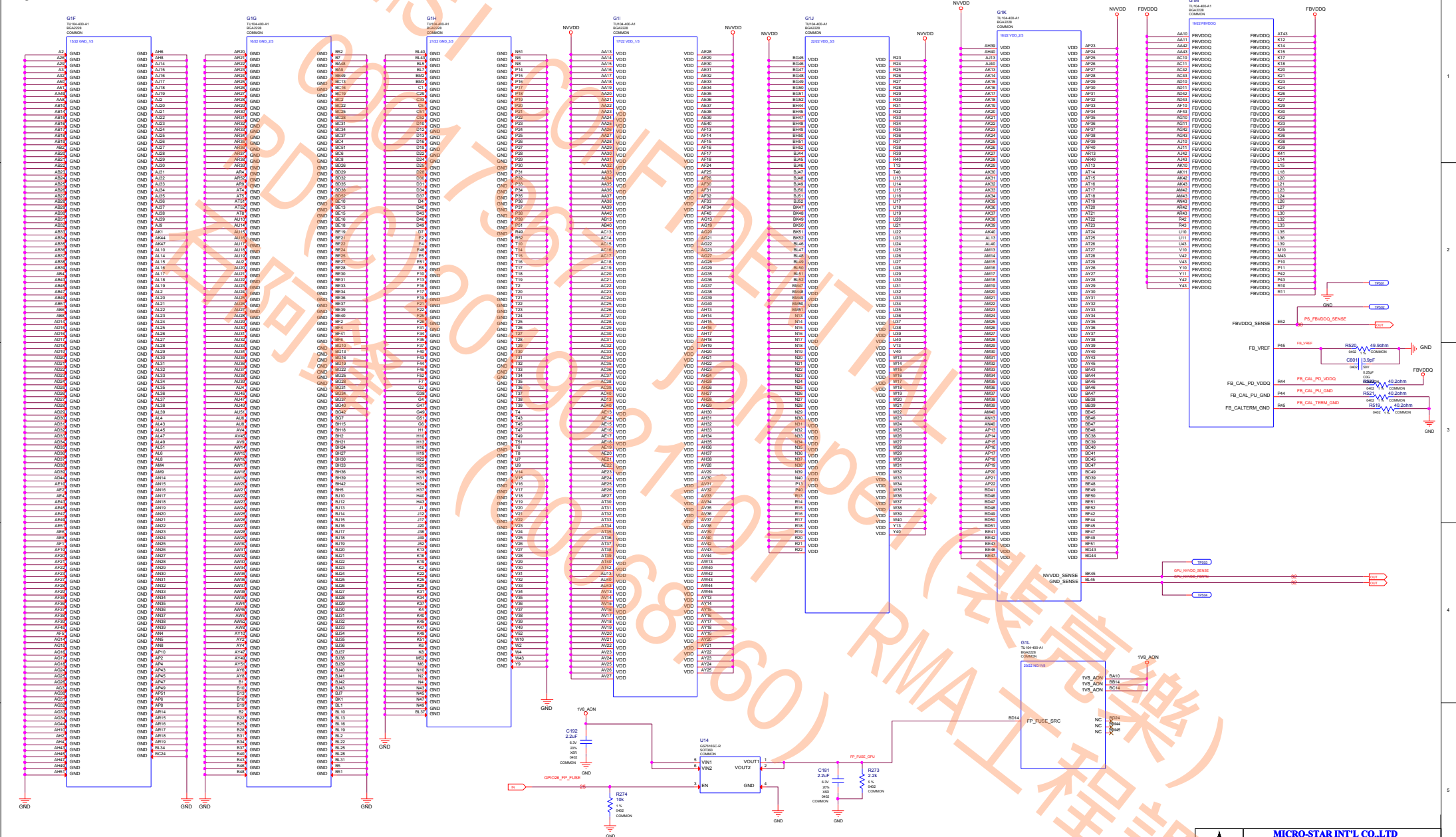






VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R62





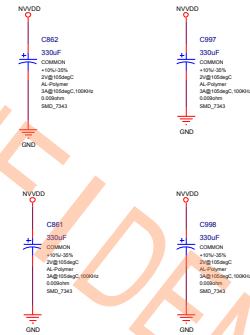
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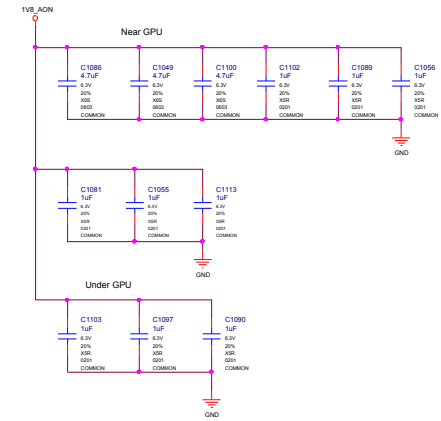
FBVDDQ



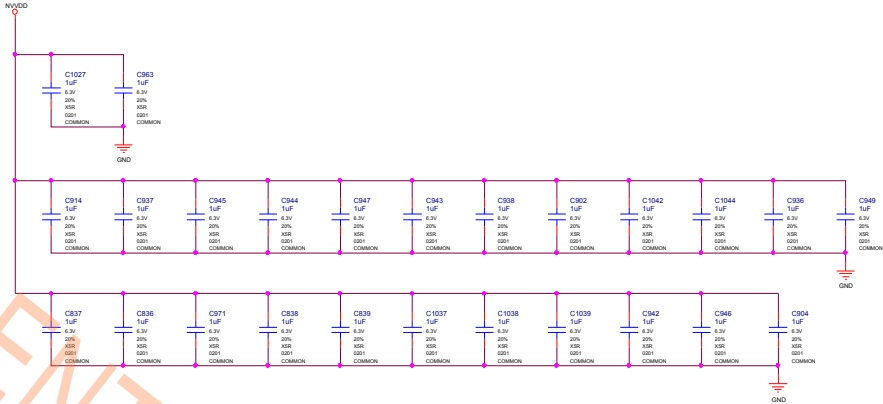
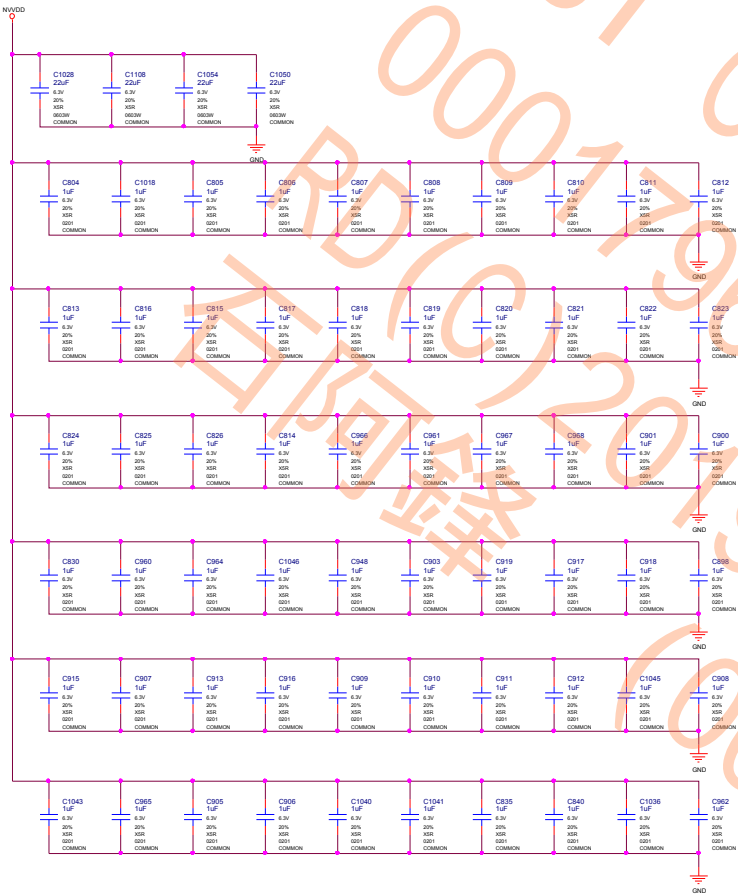
NVVD0

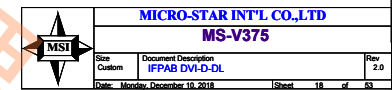


1V8_AON



NVDD



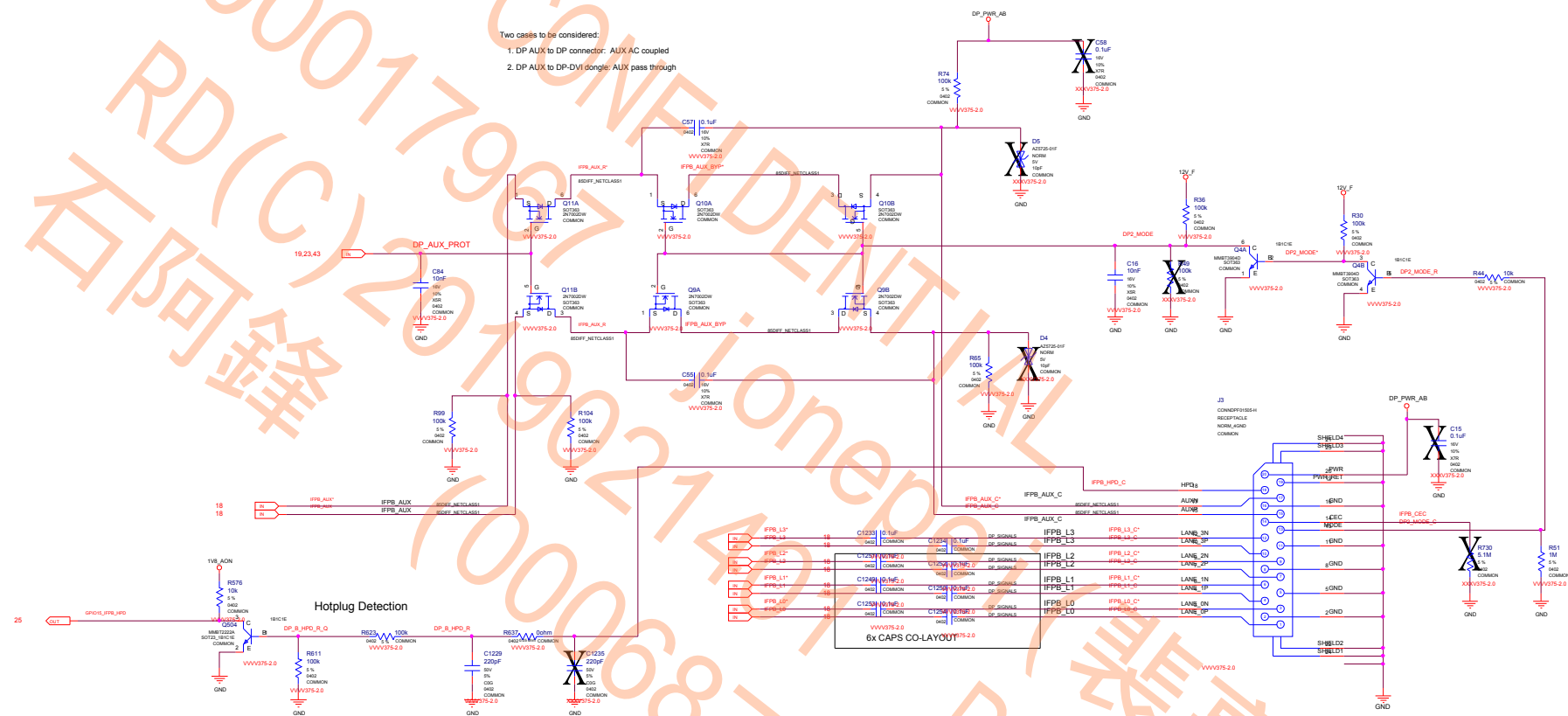




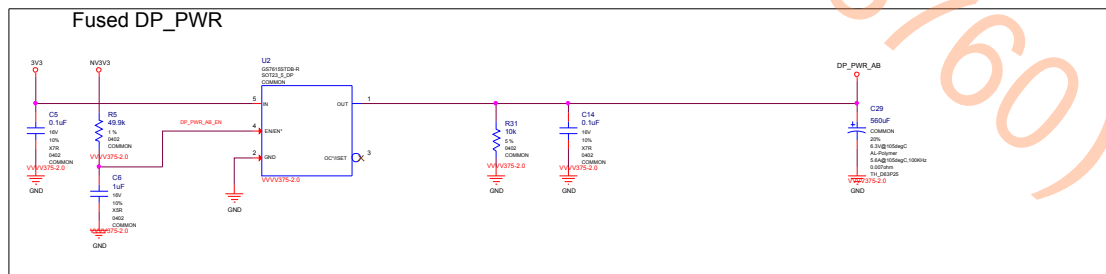
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

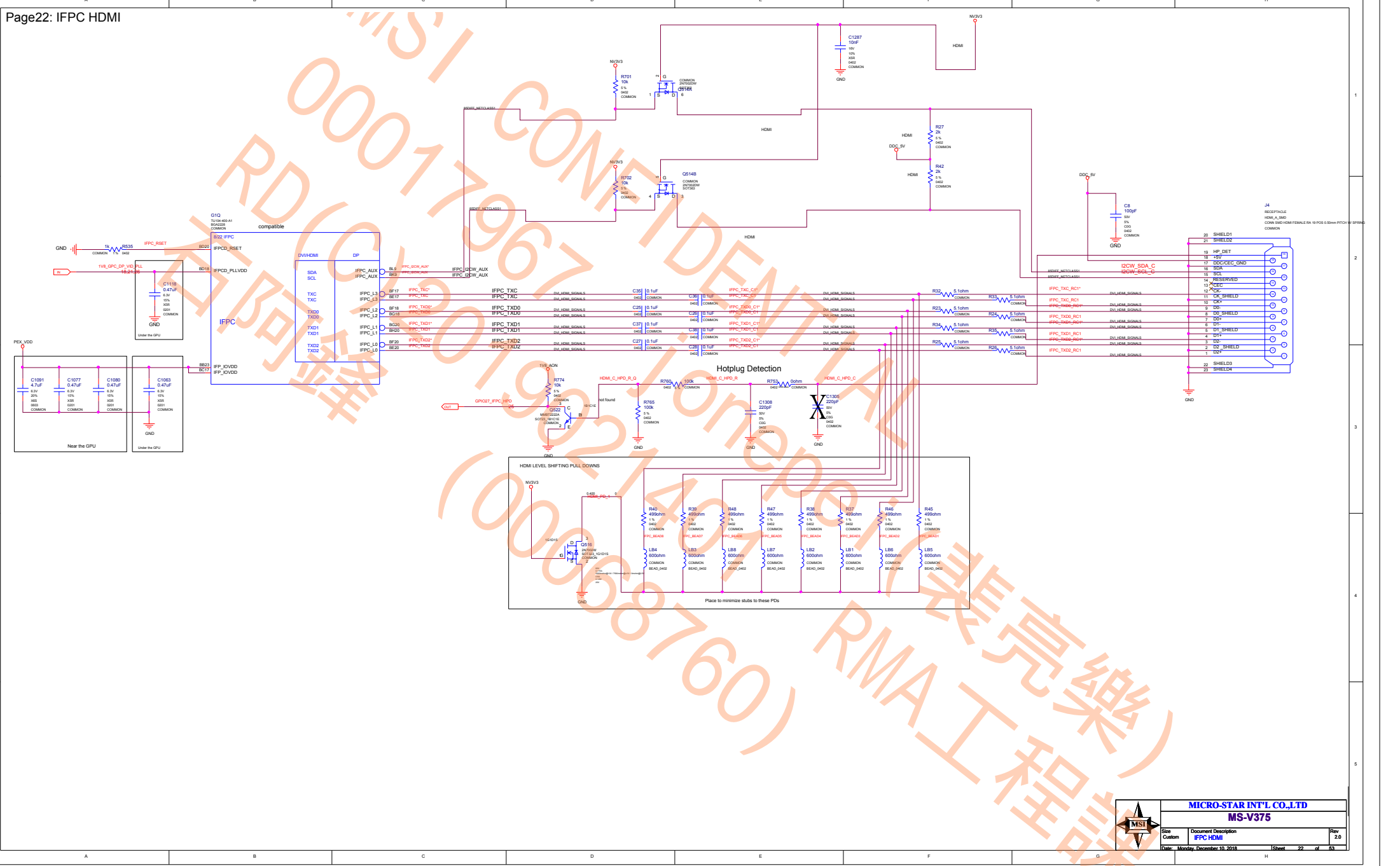


Fused DP_PWR



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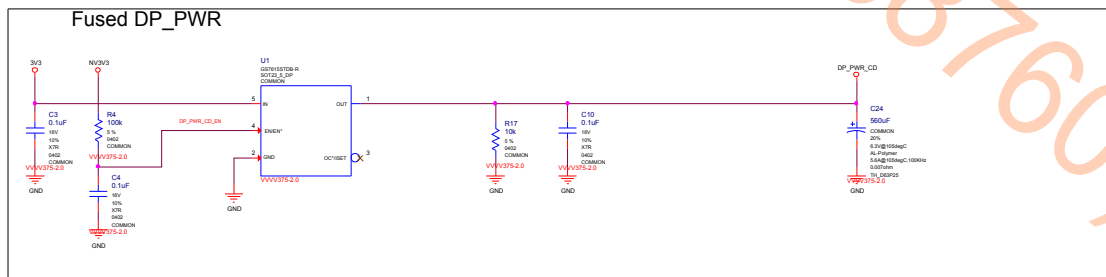
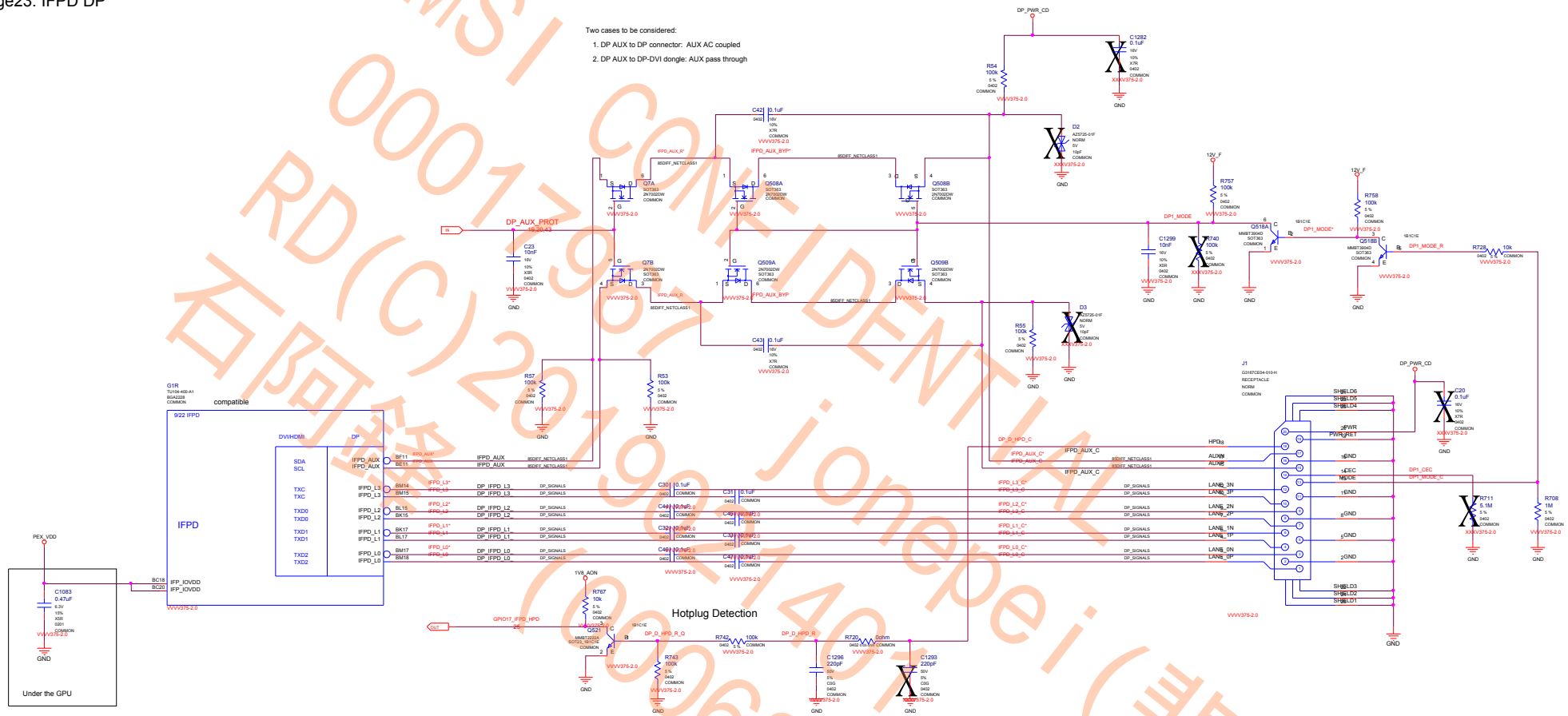
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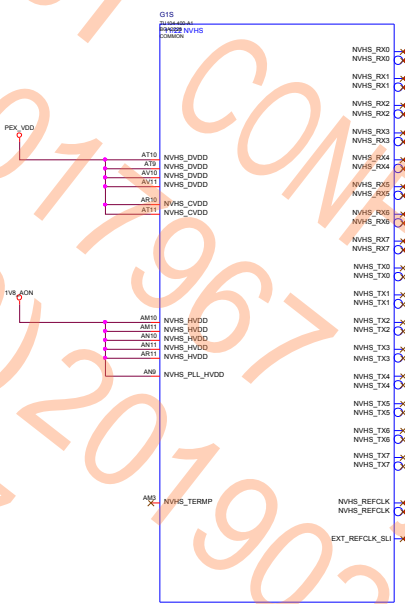
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

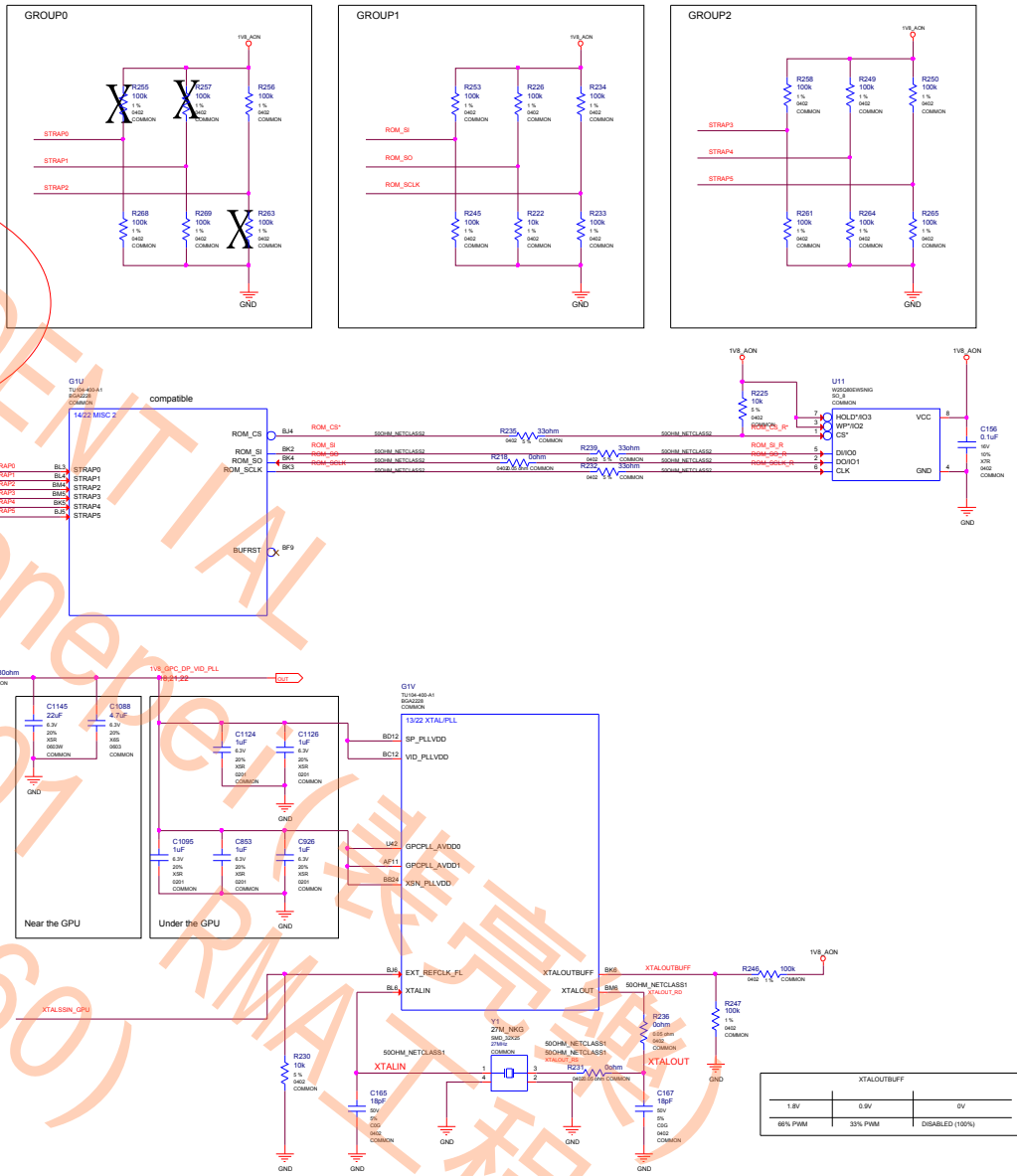
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

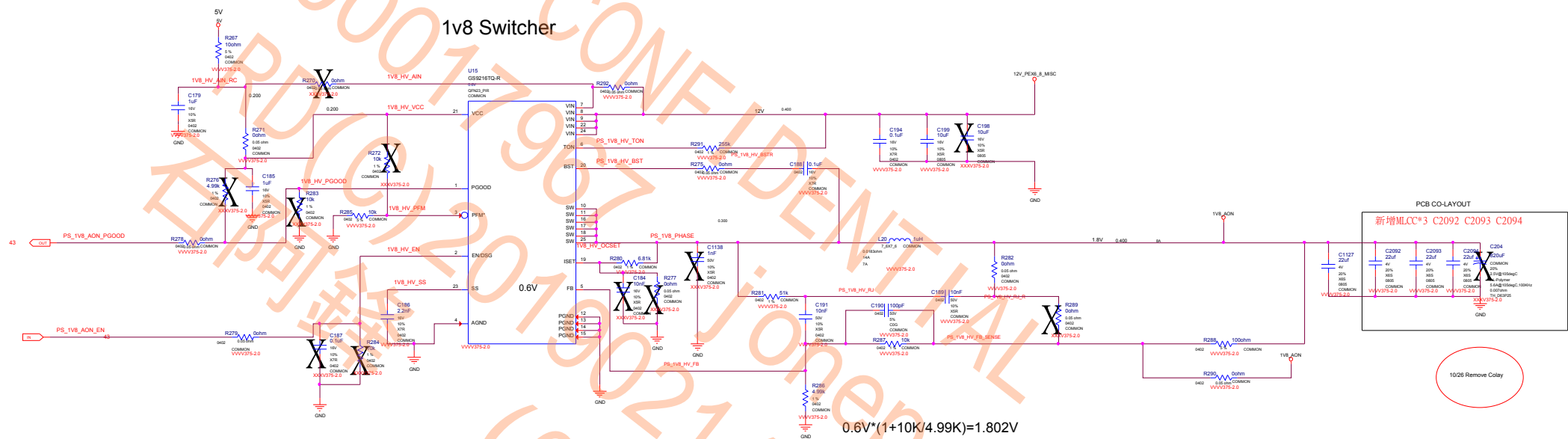
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

注意上件的MEM Straps







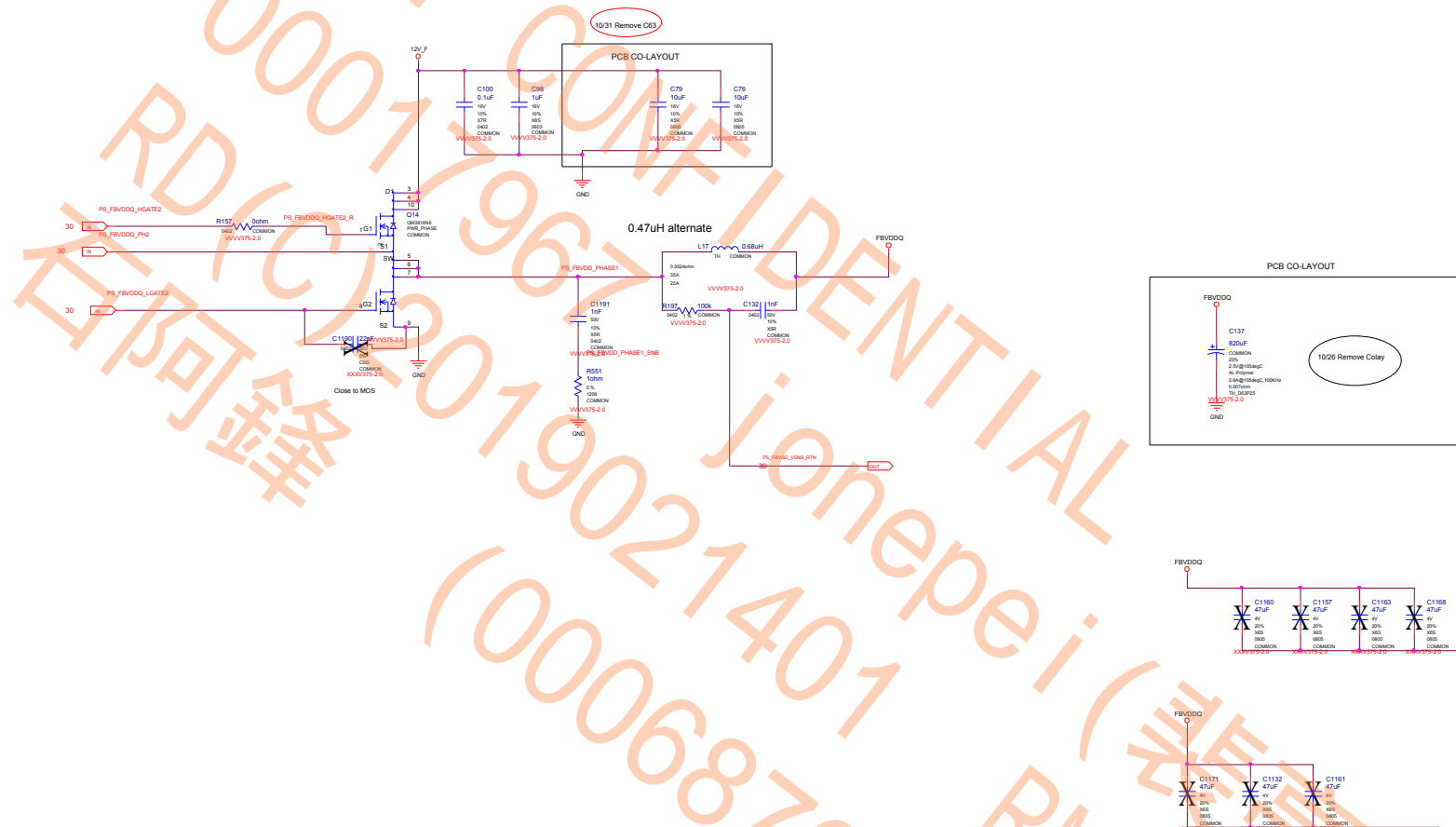
PEX Switcher

EN: $3.3V \cdot (10K/27.4K) = 1.2V$
ENABLE DISCHARGE OF PEX_VDD

$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$

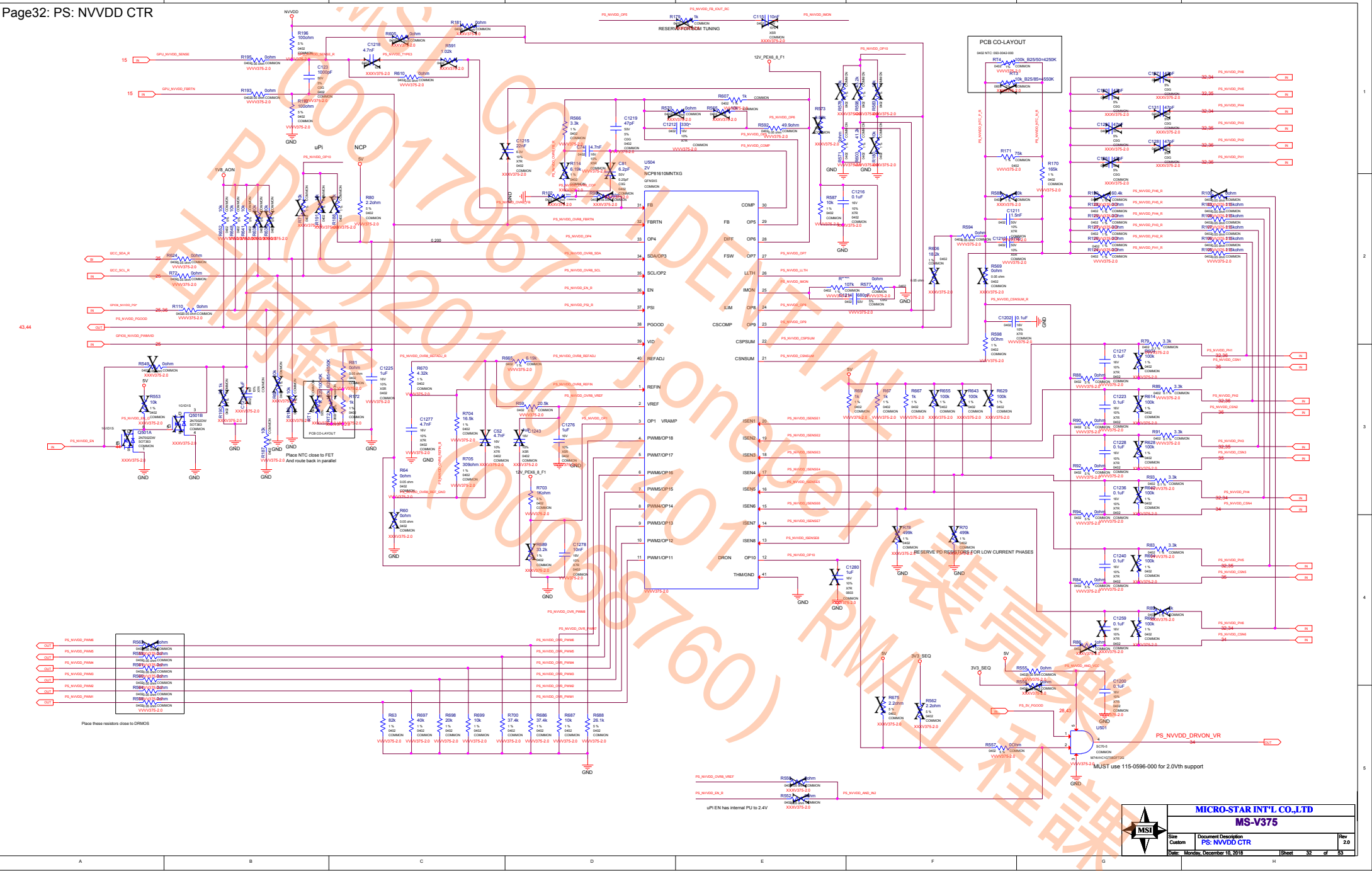
新增C2095 C2096 C2097

10/26 Remove Collay




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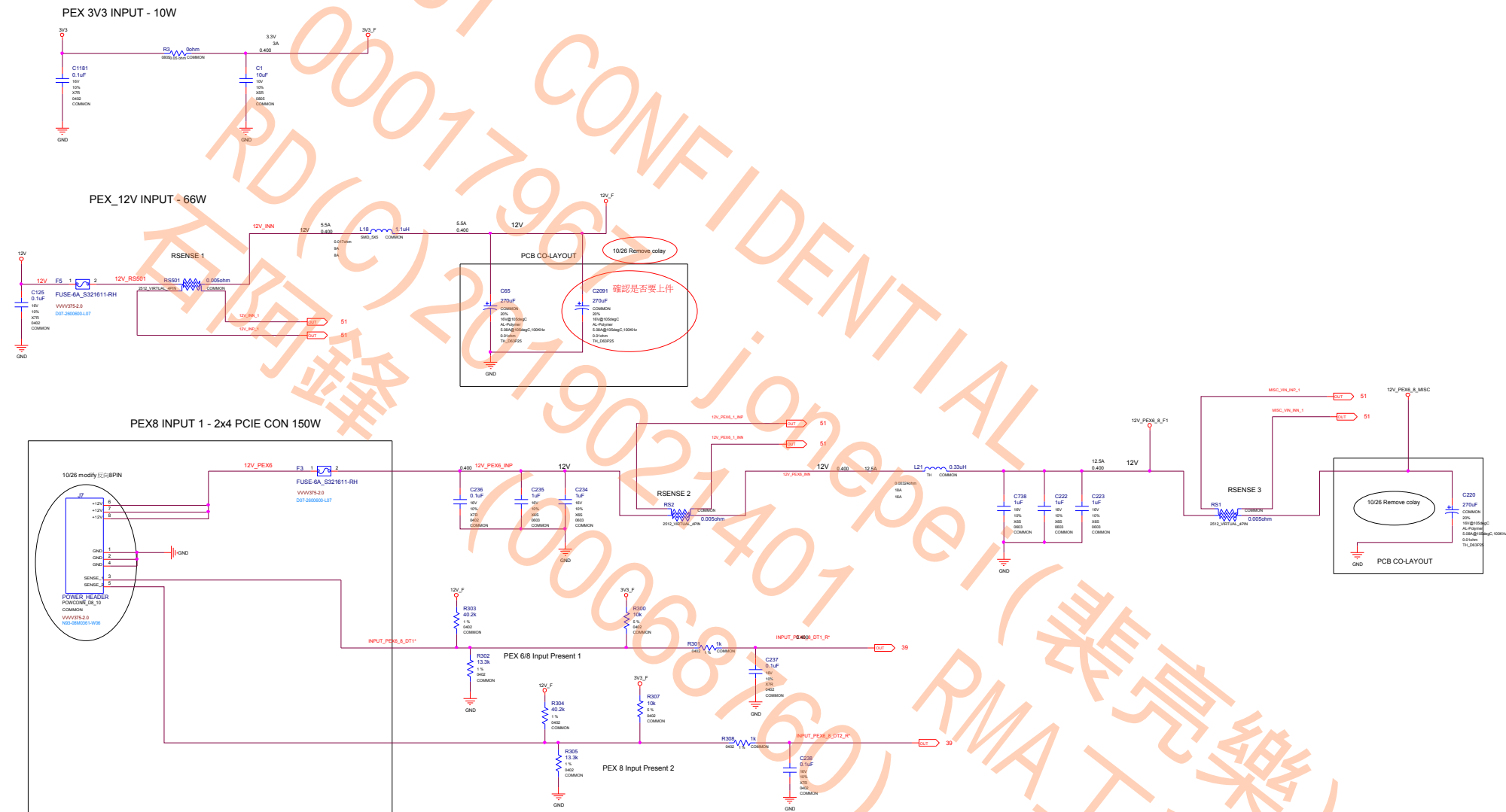


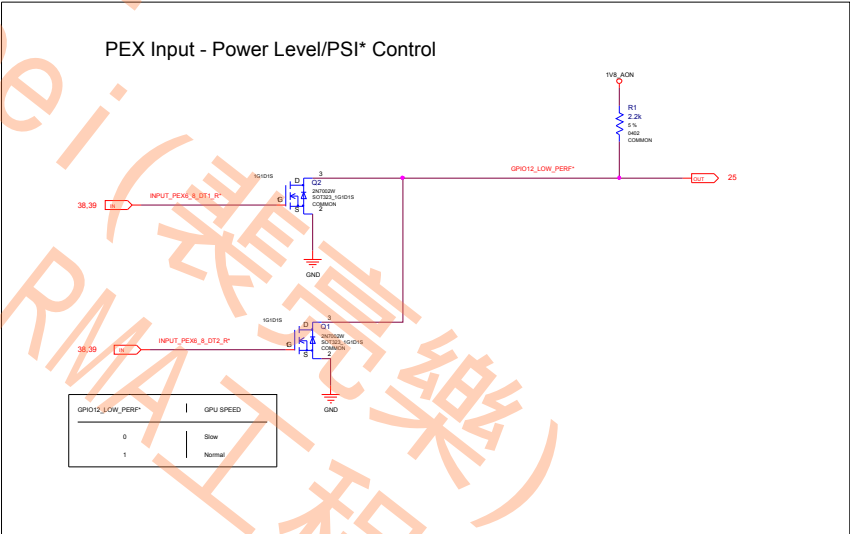
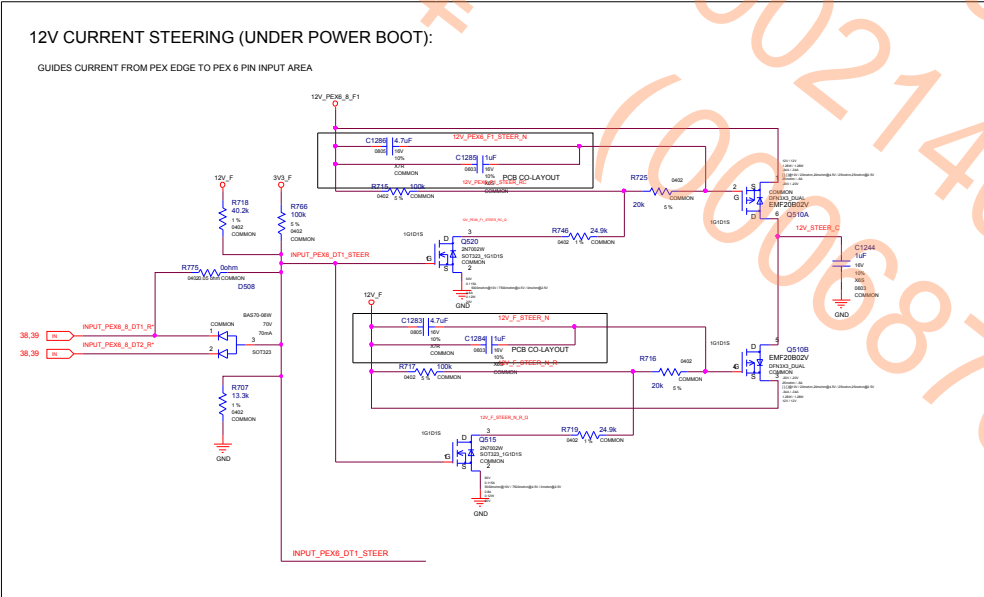
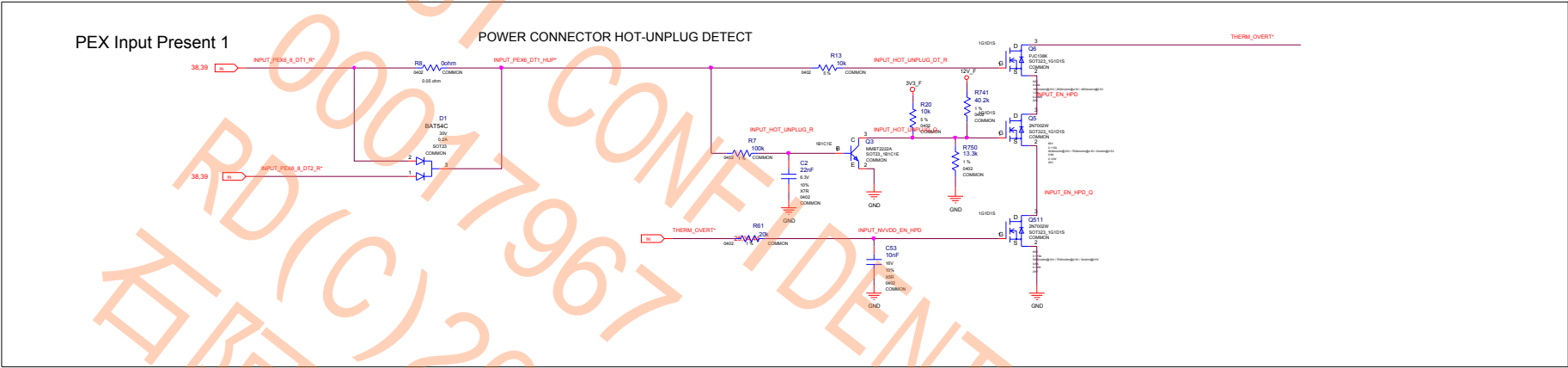
DROP OVR3i SOLUTION

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DELETE RAIL BALANCE CIRCUIT

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石阿鋒 (00068760) RMA工程師

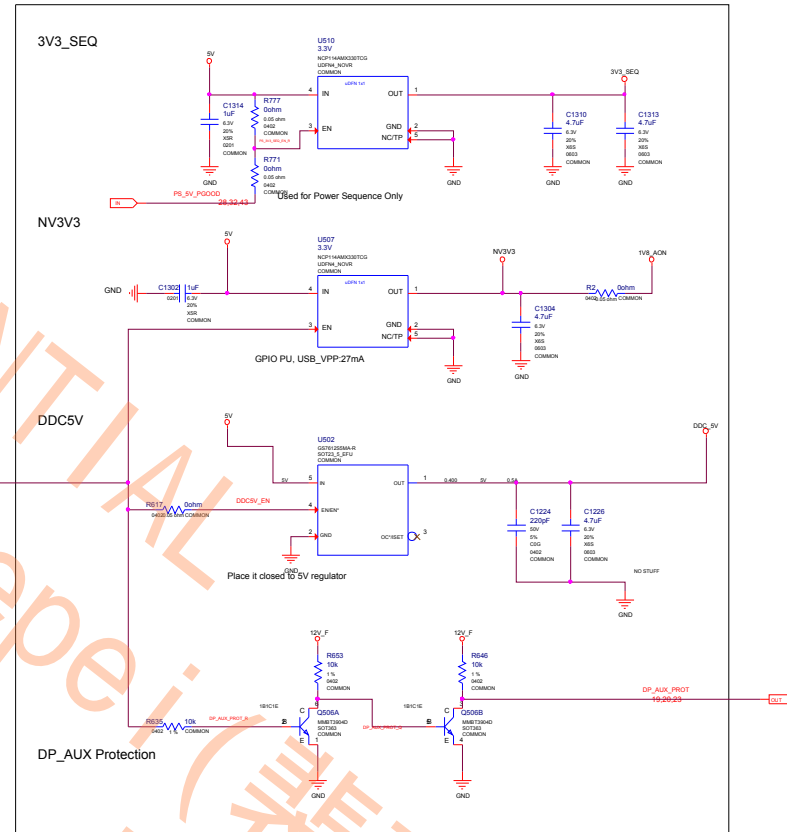
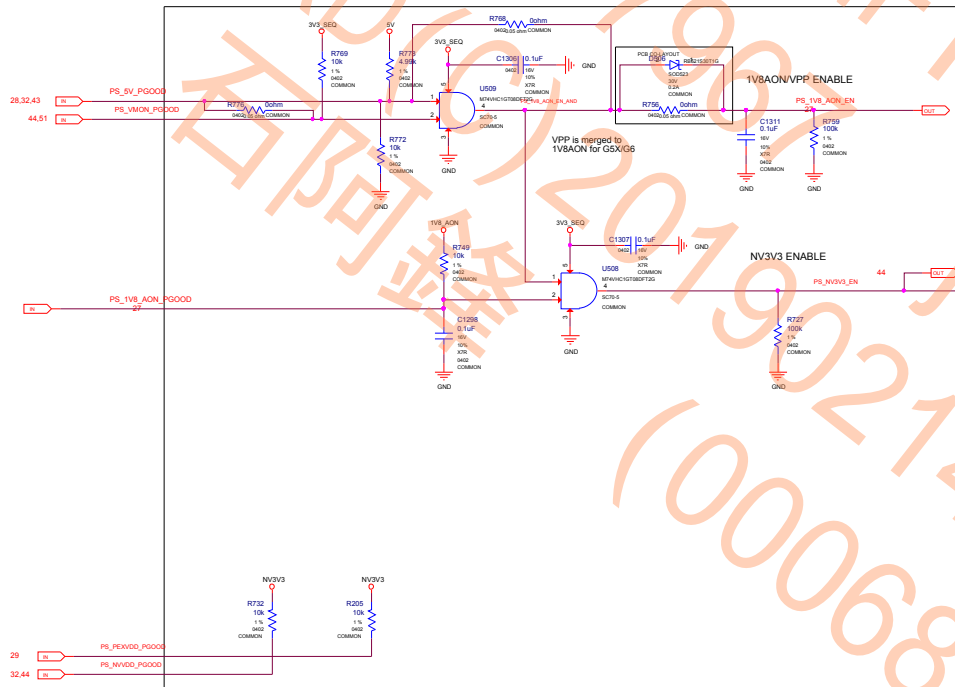
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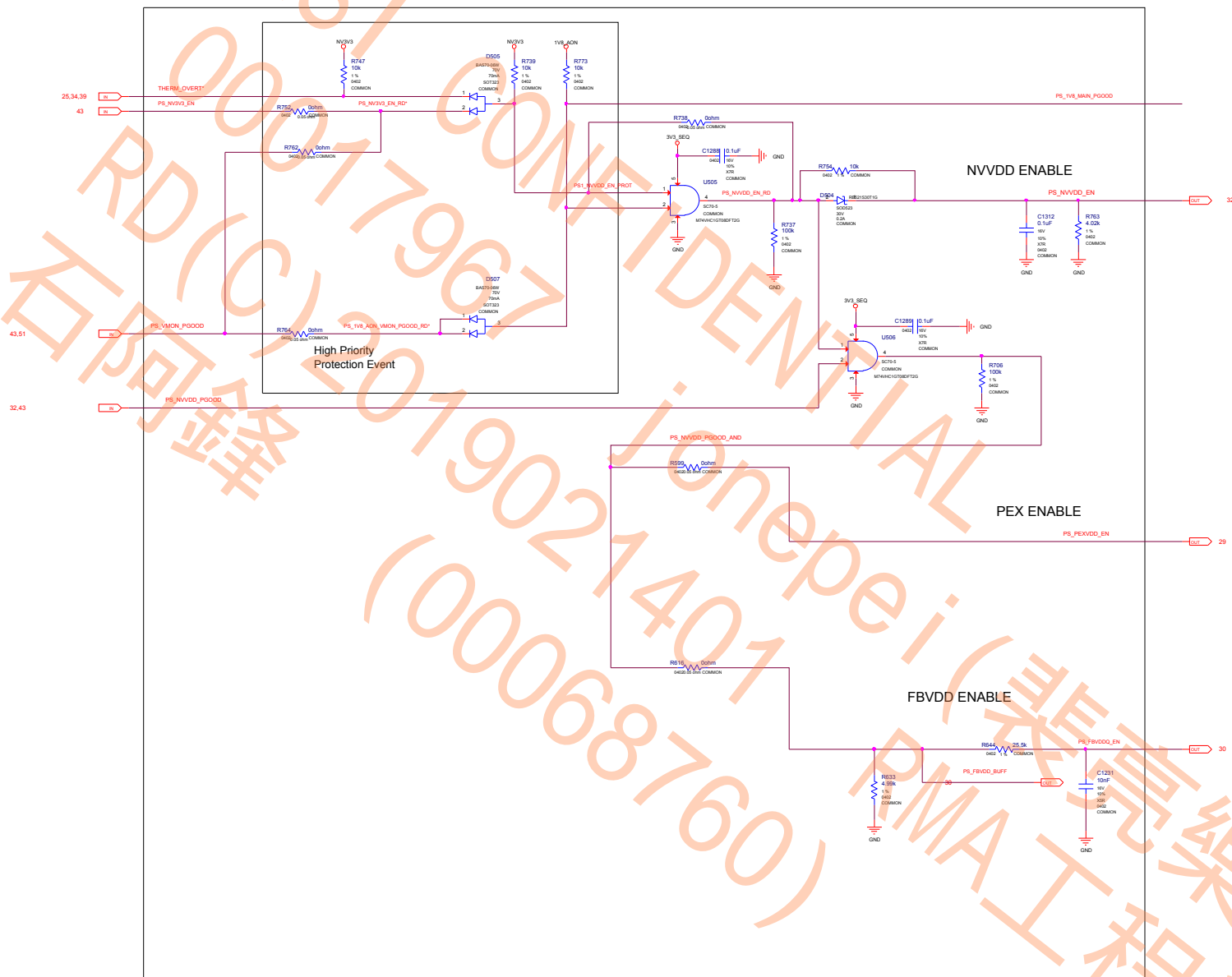
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Custom	12V & 3V3_A SWITCHER	2.0
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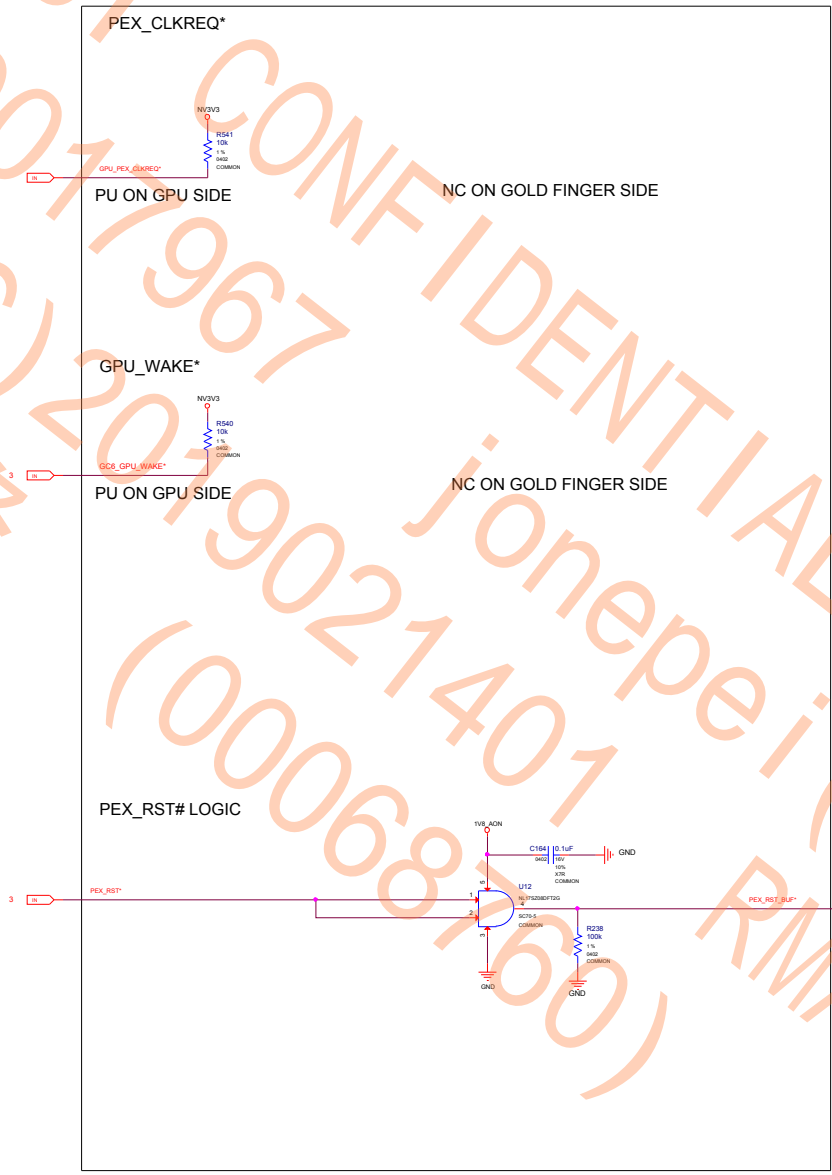
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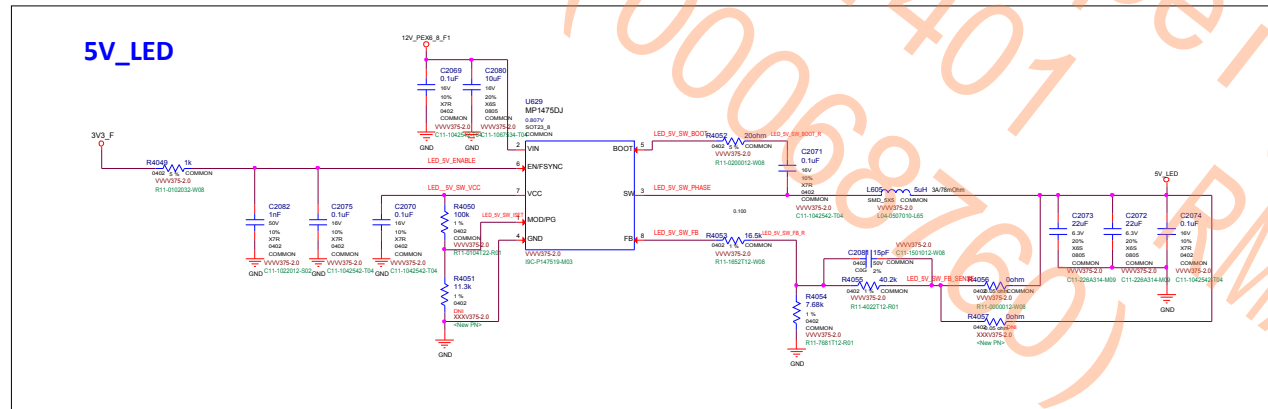
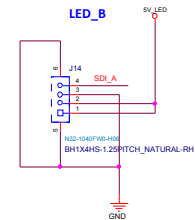
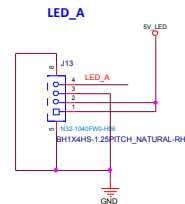
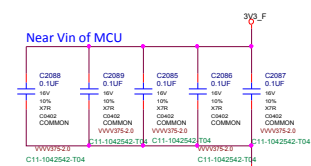
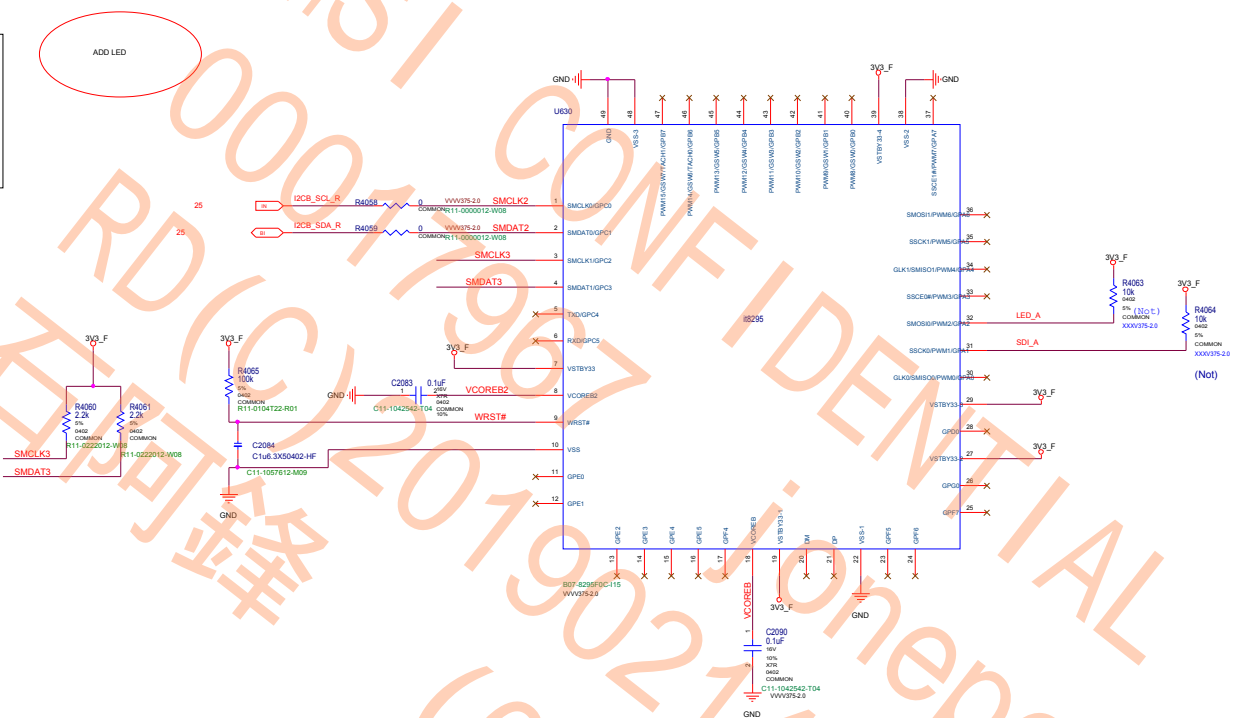
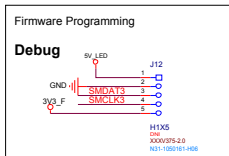
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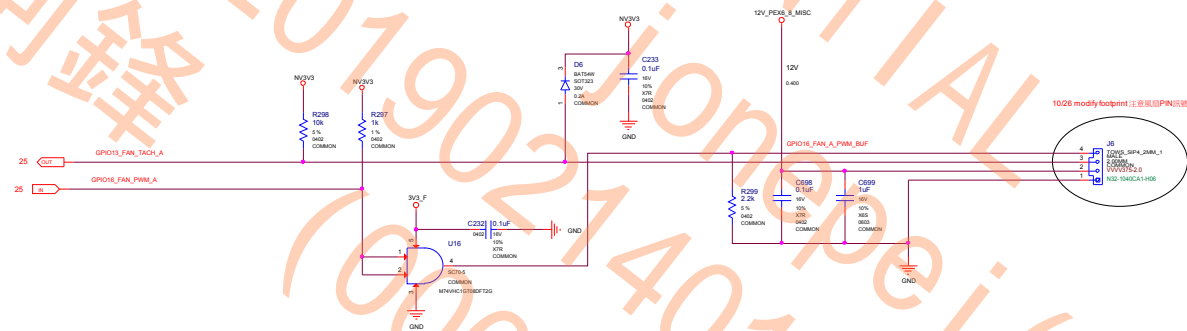
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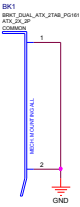
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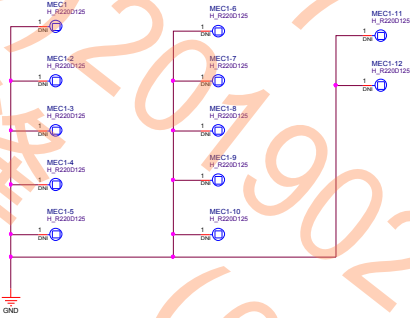




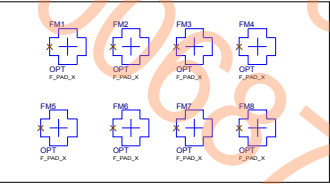
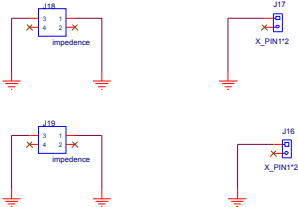
Bracket:




MOUNTING HOLES FOR HS:



BACK STIFFENER:



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